Amendments to the Claims

1.   (Currently Amended) A method of converting an analog circuit from a source technology to a target technology, comprising:

receiving the analog circuit in the source technology;

converting the analog circuit from the source technology to the target technology by analyzing the analog circuit at ~~the~~ a device level and resizing the analog circuit at the device level based on ~~the analysis~~ results of the analyzing; and

outputting the analog circuit in the target technology;

wherein the analyzing the analog circuit at the device level comprises:

determining whether a first transistor is in an off mode;

if the first transistor is not off, analyzing the first transistor;

if the first transistor is off, analyzing a second transistor symmetrical to the first transistor and propagating results of analyzing the symmetrical transistor to the first transistor.

2.   (Currently Amended) The method of claim 1, wherein the analyzing the analog circuit at the device level comprises determining a mode of operation for a transistor in the analog circuit and ~~the~~ resizing of the transistor ~~is~~ based on the determined mode of operation.

3.   (Currently Amended) The method of claim 1, wherein the analyzing the analog circuit at the-device level comprises determining node voltages coupled to a device and ~~the~~ resizing of the device ~~is~~ based on the determined node voltages.

4.   (Canceled)

5.   (Currently Amended) The method of claim 1, wherein the analyzing the analog circuit at the-device level comprises analyzing individual electrical devices, which are one or more of the following types: transistors, resistors, and capacitors.

6.   (Previously Presented) The method of claim 1, further comprising performing a dc simulation of the analog circuit in the source technology to determine electrical parameters of the analog circuit and wherein the resizing is based on the determined electrical parameters.

7.   (Currently Amended) The method of claim 1, ~~further comprising:~~
~~identifying circuit blocks within the analog circuit;~~
associating transistors with the circuit blocks; and
selecting a ~~next~~transistor to resize based, in part, on the circuit ~~block~~ blocks.

8.   (Previously Presented) The method of claim 1, wherein analyzing the analog
circuit comprises analyzing node voltages coupled to a resistor and resizing the resistor based on
the node voltages.

9.   (Currently Amended) The method of claim 1, further comprising receiving, on a
server computer, a circuit description from a client computer over a distributed network, resizing
the description on the server computer, and returning ~~the resized~~ results of the resizing to the
client computer over the distributed network.

10.   (Currently Amended) The method of ~~claim 1~~ claim 2, wherein the resizing ~~of~~ a
transistor comprises checking that changes to ~~the~~ output conductance and parasitic capacitance of
the resized transistor remain within a certain accuracy limit.

11.   (Currently Amended) A circuit retargeting system to convert an analog circuit
from a source technology to a target technology, comprising:
        a design extraction engine that determines electrical parameters associated with the
analog circuit; ~~and~~
        a resizing engine coupled to the design extraction engine that resizes individual devices
within the analog circuit using the determined electrical parameters to convert the analog circuit
from the source technology to the target technology; and
        an optimization engine coupled to the resizing engine, the optimization engine further
changing the resized analog circuit taking into account timing issues and constraints.

12.   (Canceled)

13.   (Previously Presented) The circuit retargeting system of claim 11, further comprising a simulator coupled to the design extraction engine used to obtain the electrical parameters, comprising voltage levels on nodes within the analog circuit.

14.   (Previously Presented) The circuit retargeting system of claim 11, further comprising a source technology parameter database and a target technology parameter database both coupled to the resizing engine.

15.   (Currently Amended) The circuit retargeting system of claim 11, further comprising a network comprising a client computer coupled to a server computer and wherein the circuit retargeting system is distributed over the network.

16.   (Currently Amended) The circuit retargeting system of ~~claim 11~~ claim 15, wherein the server computer receives the analog circuit in the source technology, resizes the analog circuit to the target technology, and sends the resized circuit to the client computer.

17.   (Currently Amended) The analog circuit retargeting system of claim 11, wherein the circuit is converted from the source technology to the target technology without any performance evaluation of the overall circuit.

18.   (Currently Amended) A circuit retargeting system to convert an analog circuit from a source technology to a target technology, comprising:
        means for receiving the analog circuit in the source technology;
        means for converting the analog circuit from the source technology to the target technology by analyzing the analog circuit at ~~the~~ device level and resizing the analog circuit at the device level based on ~~the analysis~~ results of the analyzing; ~~and~~
        means for outputting the analog circuit in the target technology; and
        means for optimization for further changing the resized analog circuit taking into account timing issues and constraints..

19.   (New) A method of converting an analog circuit from a source technology to a target technology, comprising:

receiving, in a computer, the analog circuit in the source technology;

converting the analog circuit from the source technology to the target technology by analyzing the analog circuit at a device level and resizing the analog circuit at the device level based on results of the analyzing by resizing substantially each transistor, resistor, and capacitor individually, rather than treating such components in blocks, which include multiple of such components; and

outputting the analog circuit in the target technology.

20.   (New) The method of claim 19, wherein the analyzing the analog circuit at the device level comprises:

determining whether a first transistor is in an off mode;

if the first transistor is not off, analyzing the first transistor;

if the first transistor is off, analyzing a second transistor symmetrical to the first transistor and propagating results of analyzing the symmetrical transistor to the first transistor.

21.   (New) The method of claim 19, wherein the analyzing the analog circuit at the device level comprises determining node voltages coupled to a device and resizing of the device based on the determined node voltages.

22.   (New) The method of claim 19, further comprising performing a dc simulation of the analog circuit in the source technology to determine electrical parameters of the analog circuit and wherein the resizing is based on the determined electrical parameters.